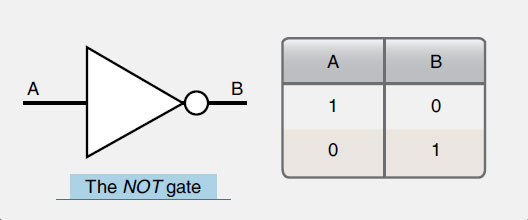
**Circuit Diagram & Truth Table:**



**Code:**

* **Design Module**

module gate(c,a);

input a;

output c;

not z(c,a);

endmodule

* **TestBench**

module test;

reg a;

wire c;

gate x(c,a);

initial

begin

a=1'b0;

#20

a=1'b1;

#20

$finish;

end

endmodule

**Output:**

